REMARKS

Applicant respectfully requests consideration of the subject application. Applicants amended claims 1, 5, 10, 16, 22, 28, 32 to better define the scope of the original claims. Thus, Applicants added no new matter.

Claim Rejections Under 35 U.S.C. §103(a)

Claims 1-4, 10-21, and 28-37

Claims 1-3, 10, 13, 14, 16, 19, 20, 28-30, 32, 35, and 36 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Gamble in view of AAPA, and further in view of Wills.

No Motivation to Combine

Applicant respectfully disagrees with the rejection because the references fail to suggest or motivate one skilled in the art to modify or combine the cited references. Moreover, one skilled in the art would not be motivated to modify or combine the references based on knowledge in the art of data communications that relates to transmission of data through multiple clock domains using synchronous and asynchronous devices.

The references fail to suggest or to motivate one skilled in the art of storing data defined by a first transmission standard in a network element and outputting the data at a second data transfer rate defined by a second transmission standard. First, Gamble describes a method and apparatus for use in a computer system

(Gamble, col. 1, ll. 9-12) unlike Wills that describes a way of transferring asynchronous transfer mode (ATM) cells from the input ports to the output ports of an asynchronous transfer mode (ATM) switch (Wills, Abstract). Specifically, Gamble describes "a method and apparatus for controlling data transfers between two interfaces of a computer system that have different rates" such as a SCSI/SCSI2 controller to a DMA controller (Gamble, col. 1, ll. 9-12, Abstract, Figure 4, emphasis added). Conversely, Wills describes an asynchronous transport mode ATM switch for transferring asynchronous transport mode (ATM) cells from input channels to output channels (Wills, Abstract). The asynchronous transport mode switch of Wills routes asynchronous transport mode cells to minimize delay and loss. (Wills, col. 1, ll. 22-24). Because the ATM switch is asynchronous, the data rate of the data contained within each ATM cell to be routed is of no significance to the ATM switch. Therefore, there is no suggesting in the references or motativation for one skilled in the art to combine these references.

Moreover, the problem solved in Gamble and Wills does not provide motivation to combine the references. Specifically, Gamble describes controlling data transfers between two interfaces of a computer system that have different data rates and matching the maximum data rate of each. (Gamble, col. 1, ll. 9-12; Gamble, Abstract). Conversely, Wills describes the probability of overwhelming an output buffer as the number of input ports are added to the asynchronous transfer mode (ATM) switch. (Wills, col. 1, ll. 38-40).

One skilled in the art of data communications that relates to transmission of data through multiple clock domains using synchronous and asynchronous devices

would not have knowledge generally available to modify or combine a reference about data transfers between two interfaces of a computer system such as a SCSI/SCSI2 controller to a DMA controller with a reference about transferring asynchronous transfer mode cells from input channels to output channels of an ATM switch. Because no motivation to combine the references exists in the references, in the nature of the problem to be solved, or in the knowledge of one of ordinary skill in the art, the combination of the references is impermissible hindsight. (MPEP § 2145).

Combinations

Claims 1 and 28

Even if the combination is maintained the combination fails to describe each and every element of claims 1 and 28. Claims 1 and 28 require storing data of a first data transfer rate defined by a first transmission standard in a synchronous storage device of a network element. Further required by claims 1 and 28 is transmitting the data of the first data transfer rate to an asynchronous storage device of the network element. Claim 1 and 28 also require that the first storage area of the synchronous storage device be larger than the second storage area of the asynchronous device. Moreover, claims 1 and 28 require outputting the data of the first data transfer rate defined by the first transmission standard from the asynchronous storage device at a second data transfer rate defined by a second transmission standard.

Gamble describes "a method and apparatus for controlling data transfers between two interfaces of a computer system that have different rates." (Gamble,

col. 1, ll. 9-12, emphasis added). Specifically, Gamble describes transferring data between computer interfaces such as a SCSI/SCSI2 controller to a DMA controller. (Gamble, Abstract and Figure 4). The transfer is accomplished by using an asynchronous FIFO and a synchronous FIFO. (Gamble, Abstract). The FIFOs are used to match the data rate of a high speed asynchronous device such as a SCSI/SCSI2 controller to a DMA controller. (Gamble, Abstract and Figure 4).

Applicants' Background of the Invention discloses the use of a synchronous FIFO when storing and transferring data within the same clock domain. Further disclosed in Applicants' Background of the Invention is the use of an asynchronous FIFO when storing and transferring data between two clock domains. This asynchronous FIFO allows for storage and extraction of data while converting the data from a first clock domain to a second domain. Control circuitry is used to control the traversal of the data through the FIFOs.

Wills describes an ATM switch for transferring ATM cells from input channels to output channels. (Wills, Abstract). Wills further describes the use of a backpressure signal circuit that sends a signal from a congested output buffer to those input port buffers which have transmitted a cell to the output buffer (during congestion) so that the input port buffers cease transmission. (Wills, Abstract).

Therefore, the combination describes a computer with the interface of Gamble including FIFOs as disclosed in Applicants' Background of the invention connected to a network including an ATM switch of Wills. Specifically, the computer includes an asynchronous FIFO and synchronous FIFO that transfers data "between two interfaces of a computer system that have different data rates" such as a

SCSI/SCSI2 controller to a DMA controller. (Gamble, col. 1, ll. 9-12, Abstract, Figure 4, emphasis added). This computer system including the interface would transmit data transported by an ATM network including the ATM switch of Wills. The ATM switch that uses a backpressure signal circuit that sends a signal from a congested output buffer to those input port buffers which have transmitted a cell to the output buffer (during congestion) so that the input port buffers cease transmission.

Because the combination does not describe storing data of a first data transfer rate defined by a transmission standard in a synchronous storage device of a network element, transmitting the data of the first data transfer rate to an asynchronous storage device of the network element, a first storage area of a synchronous storage device larger than a second storage area of an asynchronous storage device, and outputting the data of the first data transfer rate defined by the first transmission standard from the asynchronous storage device at a second data transfer rate defined by a second transmission standard, the combination fails to render claims 1 and 28 obvious.

As Applicants respectfully assert above, the combination fails to describe a first storage area of a synchronous storage device larger than a second storage area of an asynchronous device. Despite the admission that the combination is silent on the implementation of a small asynchronous FIFO, the Office Action "maintains that a 'small asynchronous FIFO' would have a storage area smaller than the synchronous FIFO since 'small' is a relative term and the only two storage units in the system of the combination of Gamble and AAPA are the asynchronous FIFO and

synchronous FIFO." If the Office Action reasserts this basis for the rejection, Applicants request clarification as to why this implies that the combination describes a first storage area of a synchronous storage device larger than a second storage area of an asynchronous device.

Claim 2-4

Applicants respectfully submit that claims 2-4 depend on independent claim 1, thus include the limitations of claim 1. As such, claims 2-4 are allowable for at least the same reasons as claim 1.

Claims 29-31

Applicants respectfully submit that claims 29-31 depend on independent claim 28, thus include the limitations of claim 28. As such, claims 29-31 are allowable for at least the same reasons as claim 28.

Claims 10 and 32

Even if the combination is maintained the combination fails to describe each and every element of claims 10 and 32. Claims 10 and 32 require receiving data at a first data transfer at a first network element of a communication system. Claims 10 and 32 also require that the first storage area of the synchronous storage device be larger than the second storage area of the asynchronous storage device. Furthermore, claim 10 and 32 requires transmitting the data out from the

asynchronous storage device at a second data transfer rate to match the data rate of a second network element.

As discussed above, the combination describes a computer with the interface of Gamble including FIFOs as disclosed in Applicants' Background of the invention connected to a network including an ATM switch of Wills. Specifically, the computer includes an asynchronous FIFO and synchronous FIFO that transfers data "between two interfaces of a computer system that have different data rates" such as a SCSI/SCSI2 controller to a DMA controller. (Gamble, col. 1, ll. 9-12, Abstract, Figure 4, emphasis added). This computer system including the interface would transmit data transported by an ATM network including the ATM switch of Wills. The ATM switch that uses a backpressure signal circuit that sends a signal from a congested output buffer to those input port buffers which have transmitted a cell to the output buffer (during congestion) so that the input port buffers cease transmission.

Because the combination does not describe receiving data at a first data transfer rate at a first network element of a communication system, a first storage area of a synchronous storage device larger than a second storage area of a asynchronous storage device, and transmitting the data out from the asynchronous storage device at a second data transfer rate to match the data rate of a second network element, the combination fails to render claims 10 and 32 obvious.

As discussed above, Applicants request clarification as to why the combination implies a first storage area of a synchronous storage device larger than a second storage area of an asynchronous storage device.

Claims 11-15

Applicants respectfully submit that claims 11-15 depend on independent claim 10, thus include the limitations of claim 10. As such, claims 11-15 are allowable for at least the same reasons as claim 10.

Claims 33-37

Applicants respectfully submit that claims 33-37 depend on independent claim 32, thus include the limitations of claim 32. As such, claims 33-37 are allowable for at least the same reasons as claim 32.

Claim 16

Even if the combination is maintained the combination fails to describe each and every element of claim 16. Claim 16 requires a synchronous storage device and an asynchronous storage device of a network element coupled with a network ring. Moreover, the synchronous storage device to store data received at a first data transfer rate defined by a transmission standard. Claim 16 also requires that the first storage area of the synchronous storage device be larger than the second storage area of the asynchronous storage device. Furthermore, claim 16 requires control circuitry to output the data from the asynchronous storage device at a second data transfer rate defined by a second transmission standard.

As discussed above, the combination describes a computer with the interface of Gamble including FIFOs as disclosed in Applicants' Background of the invention

connected to a network including an ATM switch of Wills. Specifically, the computer includes an asynchronous FIFO and synchronous FIFO that transfers data "between two interfaces of a computer system that have different data rates" such as a SCSI/SCSI2 controller to a DMA controller. (Gamble, col. 1, ll. 9-12, Abstract, Figure 4, emphasis added). This computer system including the interface would transmit data transported by an ATM network including the ATM switch of Wills. The ATM switch that uses a backpressure signal circuit that sends a signal from a congested output buffer to those input port buffers which have transmitted a cell to the output buffer (during congestion) so that the input port buffers cease transmission.

Because the combination does not describe a synchronous storage device and an asynchronous storage device of a network element coupled with a network ring, the synchronous storage device to store data received at a first data transfer rate defined by a communications transmission standard, a first storage area of a synchronous storage device larger than a second storage area of an asynchronous storage device, and control circuitry to output the data from the asynchronous storage device at a second data transfer rate defined by a second communication transmission standard, the combination fails to render claim 16 obvious.

As discussed above, Applicants request clarification as to why the combination implies a first storage area of a synchronous storage device larger than a second storage area of an asynchronous storage device.

Claims 17-21

Applicants respectfully submit that claims 17-21 depend on independent claim 16, thus include the limitations of claim 16. As such, claims 17-21 are allowable for at least the same reasons as claim 16.

Claims 25-27

Claims 25-27 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Gamble in view of Wills, Subrahmanyan, and further in view of Newton, "Newton's Telecom Dictionary", Oct. 1998, Telecom Books, pgs. 535 and 732 ("Newton").

No Motivation to Combine

As discussed above, Gamble and Wills fail to suggest or motivate one skilled in the art of data communications that relates to transmission of data through multiple clock domains using synchronous and asynchronous devices to modify or combine the cited references. Likewise, one skilled in the art of data communications that relates to transmission of data through multiple clock domains using synchronous and asynchronous devices would not be motivated to modify or combine the references of Gamble and Wills. Because no motivation to combine the references exist in the nature of the problem to be solved or in the knowledge of one of ordinary skill in the art of data communications that relates to transmission of data through multiple clock domains using synchronous and asynchronous devices, the combination of the references is impermissible hindsight. (MPEP § 2145).

Furthermore, no suggestion or motivation to combine with Gamble or Wills

exists in Subrahmanyan. Subrahmanyan describes the problem of reducing the effects of pointer adjustments, wander, and jitter during desynchronization and recovery of a payload data stream from a synchronized signal in a synchronous communications network such as SONET or SDH. (Subrahmanyan, paras. [0001] and [0024]). No suggestion or motivation exists in Subrahmanyan to combine with Gamble, dealing with controlling data transfers between two interfaces of a computer system that have different data rates and matching the maximum data rate of each. (Gamble, col. 1, ll. 9-12, Abstract). Similarly, no suggestion or motivation exists in Subrahmanyan to combine with Wills, dealing with the probability of overwhelming an output buffer as the number of input ports are added to the asynchronous transfer mode (ATM) switch. (Wills, col. 1, ll. 38-40). Because Subrahmanyan, Gamble, and Wills solve different problems, there is no motivation to combine the references existent in the nature of the problems. Moreover, one skilled in the art of data communications that relates to transmission of data through multiple clock domains using synchronous and asynchronous devices would not the motivation to combine the references based on the knowledge in the art because the references solve different problems in different technology areas.

Because no motivation to combine the references exists in the references, in the nature of the problem to be solved, or in the knowledge of one of ordinary skill in the art of data communications that relates to transmission of data through multiple clock domains using synchronous and asynchronous devices, the combination of the references is impermissible hindsight. (MPEP § 2145).

Combinations

Claim 25

Even if the combination is maintained the combination fails to describe each and every element of claim 25. Claim 25 requires a synchronous first-in-first-out register array (FIFO) coupled to receive data based on a Data Signal (DS)-3 standard from a payload of Synchronous Optical Network (SONET) frames. Claim 25 also requires that the first storage area of the synchronous first-in-first-out register array (FIFO) be larger the second storage area of the asynchronous FIFO. Moreover, claim 25 requires control circuitry to output the data from the asynchronous FIFO at a DS-3 data rate on a T3 signal.

As discussed above Gamble describes a method and apparatus for transferring data between two interfaces of a computer system that have different rates. Wills, as discussed above describes a describes an ATM switch for transferring ATM cells from input channels to output channels based on a backpressure signal circuit.

Subrahmanyan describes a method and apparatus for providing a more uniformly gapped data stream from non-uniformly gapped data extracted from a synchronous signal. (Subrahmanyan, para. [0045]). A de-framer removes overhead data bytes from a SONET/SDH message leaving gaps in the data at locations corresponding to the overhead bytes. (Subrahmanyan, para. [0043]). The removal of the bytes leaves non-uniformly distributed gaps. (Subrahmanyan, para. [0043]). Therefore, Subrahmanyan discloses an apparatus that utilizes a combination of two pointer adjustment signals embedded in the synchronized signal, such as

SONET/SDH, to determine a bit leak rate of bits from an elastic store following a pointer adjustment event such that the elastic store provides as an output a more-uniformly-distributed-gapped data stream. (Subrahmanyan, Abstract and para. [0036].

Therefore, the combination describes a computer with the interface of Gamble connected to a network including an ATM switch of Wills that includes an apparatus for providing a more uniformly gapped data stream from non-uniformly gapped data extracted from a synchronous input on the ATM as defined by Newton. Specifically, the computer includes an asynchronous FIFO and synchronous FIFO that transfers data "between two interfaces of a computer system that have different data rates" such as a SCSI/SCSI2 controller to a DMA controller. (Gamble, col. 1, ll. 9-12, Abstract, Figure 4, emphasis added). This computer system including the interface would transmit data transported by an ATM network including the ATM switch of Wills. The ATM switch that uses a backpressure signal circuit that sends a signal from a congested output buffer to those input port buffers which have transmitted a cell to the output buffer (during congestion) so that the input port buffers cease transmission. The asynchronous transfer mode (ATM) switch having a synchronous input such as SONET/SDH. This SONET/SDH input could be an OC-N signal as defined in Newton. The synchronous input including a de-framer that removes overhead bytes from the synchronous messages received through the synchronous input leaving non-uniformly distributed gaps in the synchronous message. The combination further including an apparatus that utilizes a combination of two pointer adjustment signals embedded in the synchronized signal

to determine a bit leak rate of bits from an elastic store following a pointer adjustment event such that the elastic store provides as an output a more-uniformly-distributed-gapped data stream.

Because the combination does not describe a synchronous first-in-first-out register array (FIFO) coupled to receive data based on a Data Signal (DS)-3 standard from a payload of Synchronous Optical Network (SONET) frames, a first storage area of a synchronous FIFO larger than a second storage area of an asynchronous FIFO, and control circuitry to output the data from the asynchronous FIFO at a DS-3 data rate on a T3 signal, the combination fails to render claim 25 obvious.

As discussed above, Applicants request clarification as to why the combination implies a first storage area of a synchronous FIFO larger than a second storage area of an asynchronous FIFO.

Claims 26-27

Applicants respectfully submit that claims 26-27 depend on independent claim 25, thus include the limitations of claim 25. As such, claims 26-27 are allowable for at least the same reasons as claim 25.

Claims 22-24 and 38-40

Claims 22-24 and 38-40 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Gamble in view of Subrahmanyan, Wills, and further in view of Newton.

No Motivation to Combine

As discussed under claims 25-27, no motivation to combine the references exists in the references, in the nature of the problem to be solved, or in the knowledge of one of ordinary skill in the art of data communications that relates to transmission of data through multiple clock domains using synchronous and asynchronous devices; therefore, the combination of the references is impermissible hindsight. (MPEP § 2145).

Combinations

Claims 22 and 38

Even if the combination is maintained the combination fails to describe each and every element of claims 22-38. Claims 22 and 38 requires receiving data based on a Data Signal (DS)-3 standard from a payload of Synchronous Optical Network (SONET) frames. Moreover, claims 22 and 38 requires extracting the data based on the DS-3 standard from the payload of the SONET frames. Claims 22 and 38 also require that the first storage area of the synchronous first-in-first-out register array (FIFO) be larger than the second storage area of the asynchronous FIFO. A further requirement of claims 22-38 includes outputting the data based from the asynchronous FIFO at a DS-3 data rate on a T3 signal.

As discussed above, the combination describes a computer with the interface of Gamble connected to a network including an ATM switch of Wills that includes an apparatus for providing a more uniformly gapped data stream from non-uniformly

gapped data extracted from a synchronous input on the ATM as defined by Newton. Specifically, the computer includes an asynchronous FIFO and synchronous FIFO that transfers data "between two interfaces of a computer system that have different data rates" such as a SCSI/SCSI2 controller to a DMA controller. (Gamble, col. 1, ll. 9-12, Abstract, Figure 4, emphasis added). This computer system including the interface would transmit data transported by an ATM network including the ATM switch of Wills. The ATM switch that uses a backpressure signal circuit that sends a signal from a congested output buffer to those input port buffers which have transmitted a cell to the output buffer (during congestion) so that the input port buffers cease transmission. The asynchronous transfer mode (ATM) switch having a synchronous input such as SONET/SDH. This SONET/SDH input could be an OC-N signal as defined in Newton. The synchronous input including a de-framer that removes overhead bytes from the synchronous messages received through the synchronous input leaving non-uniformly distributed gaps in the synchronous message. The combination further including an apparatus that utilizes a combination of two pointer adjustment signals embedded in the synchronized signal to determine a bit leak rate of bits from an elastic store following a pointer adjustment event such that the elastic store provides as an output a more-uniformly-distributed-gapped data stream.

Because the combination does not describe receiving data based on a Data Signal (DS)-3 standard from a payload of Synchronous Optical Network (SONET) frames, extracting the data based on the DS-3 standard from the payload of the SONET frames, a first storage area of a synchronous FIFO larger than a second

storage area of a asynchronous FIFO, and outputting the data based from the asynchronous FIFO at a DS-3 data rate on a T3 signal, the combination fails to render claims 22 and 38 obvious.

As discussed above, Applicants request clarification as to why the combination implies a first storage area of a synchronous FIFO larger than a second storage area of an asynchronous FIFO.

Claims 23-24

Applicants respectfully submit that claims 23-24 depend on independent claim 22, thus include the limitations of claim 22. As such, claims 23-24 are allowable for at least the same reasons as claim 22.

Claims 39-40

Applicants respectfully submit that claims 39-40 depend on independent claim 38, thus include the limitations of claim 38. As such, claims 39-40 are allowable for at least the same reasons as claim 38.

Claims 5-9

Claims 5-7 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Gamble, U.S. Patent No. 5,592,629 ("Gamble") in view of Applicants' admitted prior art ("AAPA").

Claim 5

Applicant respectfully disagrees with the rejection because the combination of Gamble in view of AAPA does not describe or suggest each and every element of the invention as claimed in claim 5.

Claim 5 requires a synchronous storage device and an asynchronous storage device of a network element coupled with a network ring. Moreover, claim 5 requires the synchronous storage device to store data received at a first data transfer rate defined by a transmission standard. Furthermore, claim 5 requires control circuitry to output the data from the asynchronous storage device at a second data transfer rate defined by a second transmission standard.

As discussed above, the combination of Gamble and the FIFOs disclosed in Applicant's Background of the Invention describes an asynchronous FIFO with control circuitry to control the traversal of data through the asynchronous FIFO connected to a synchronous FIFO with control circuitry to control the transversal of data through the synchronous FIFO. The combination of this asynchronous FIFO and synchronous FIFO transfers data "between two interfaces of a computer system that have different data rates" such as a SCSI/SCSI2 controller to a DMA controller. (Gamble, col. 1, ll. 9-12, Abstract, Figure 4, emphasis added).

Because the combination does not describe a synchronous storage device and an asynchronous storage device of a network element coupled with a network ring, the synchronous storage device to store data received at a first data transfer rate defined by a transmission standard, and control circuitry to output the data from the asynchronous storage device at a second data transfer rate defined by a second transmission standard, the combination fails to render claim 5 obvious.

Claims 6-9

Applicants respectfully submit that claims 6-9 depend on independent claim 5, thus include the limitations of claim 5. As such, claims 6-9 are allowable for at least the same reasons as claim 5.

Conclusion

If the allowance of these claims could be facilitated by a telephone conference, the Examiner is invited to contact the undersigned at (408) 720-8300. If there are any additional charges, please charge our Deposit Account No. 02–2666.

Respectfully submitted,

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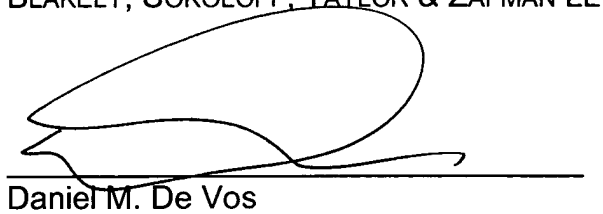

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